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國家實驗研究院

Example for TSRI Report

台灣半導體研究中心

CISD

Note

- 為讓審查會更具公平性，不可於投影片(含logo)和審查報告過程中提及申請者相關之學校系所、指導教授、實驗室、身份等資料。
- 審查過程以下線之申請編號表示案件。
- 若因違反規定造成負面審查結果，需自行負責!
- 投影片格式，頁數不拘，以重點敘述為主。但內容必需包含以下範例所提及項目(範例均為審查委員經常詢問項目)
- 投影片請務必加上頁碼，以利委員審查與提問。

審查會報告 範例

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鎖相迴路於脈波產生器之設計（中文專題名稱）
Design on phase locked loops for clock generator（英文專題名稱）

申請編號: SiG-094A-A0023

Date: 2023/11/1 (日期)

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Outline

- Introduction & Motivation
  (Including last three taped-out chip records)
- Architecture & Schematic
- Simulated Results
- Layout
- Specification Table
- Measured Considerations
  (Including instrument/measure Env. setup)
- References

Introduction & Motivation

- The last three taped-out chip records

Chip number (IC編號)	Project Name	Result/status
T18-93A-XX	**XXXXXX**	**Fail/ Work/ Partial work**
T18-93C-XX	**YYYYYY**	**going on****
none***		

** if you don't get the chip yet, fill in "going on"

*** if you don't have any chip implementation record, just to fill in "none"

- List motivations for this PLL.
- List contributions (feature) for this PLL.

Architecture & Schematic

- All schematic of PLL must be revealed clearly. (need to detail describe it during presentation.)

- Design principle of this new PLL can be explained briefly.

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Simulated Results

- Simulated results/figures of this PLL must include all corner cases of process.
- Simulated results/figures of this PLL must be shown clearly.
- All parameter which need to measure must be description clearly.

Layout

- The layout of this PLL must be clearly revealed. (It’s important for RF circuit)

- Clear node-notation in layout for this PLL is necessary.

Specification Table

- Table list all specifications of this PLL and point out which need to measured.

Item	Specification (unit)	measure
Vdd (Supply voltage)	3.3 V	N/A
Kvco	60 MHz/V	Yes
Phase Noise	-98 dBc @ 1MHz	Yes
Locking time	22 us	Yes
Jitter	430 ps	Yes
Power Consumption	11 mW	Yes
Chip Area	1500 X 1500 um^2	N/A
…..		

Measured Considerations

- List all measured instruments you need, and illustrate those purpose.
- List measure setup for each parameter you need to know.
- Mark where you will measure.

  (in CIC, NDL, self's Lab., et al….)

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References

- [1] Donhee Ham, Ali Hajimiri, “Concepts and Methods in Optimization of Integrated LC VCOs, ” IEEE Journal of Solid-State Circuits, Vol. 36 No.6, pp.896-909, June 2001.
- [2] ….