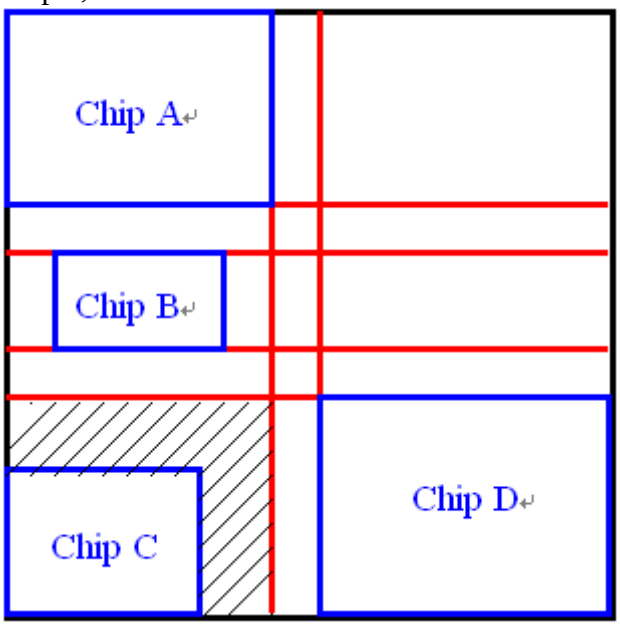
Chip Arrangement Techniques and Precautions:

Since the TSRI-proposed CMOS process dicing method involves entrusting manufacturers with a diamond knife for destructive dicing, MPW's overall chip layout arrangement requires the use of a diamond knife for destructive dicing. It implies that multi-path or segmented dices cannot be made in a single stroke, so dicing lanes must be reserved for dicing purposes.

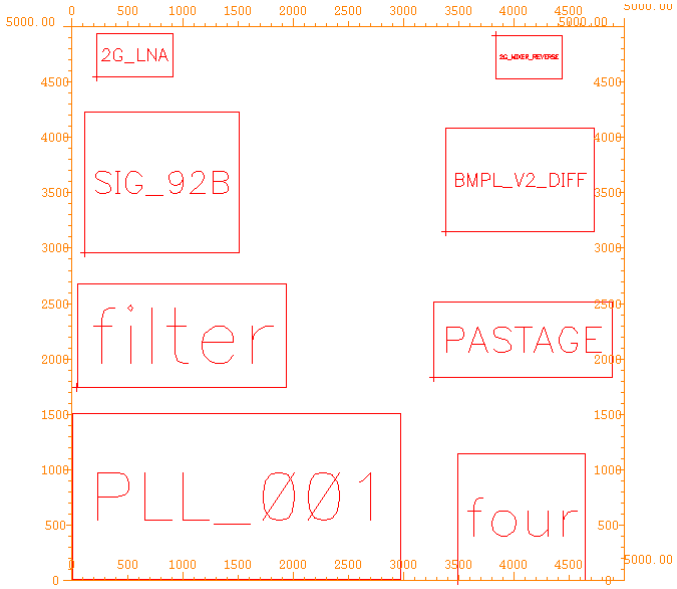
When schools entrust TSRI with the chip manufacturing through self-payment, the chip dicing lane is **200 um**. When taking shuttle, a dicing lane does not need to be reserved in the boundaries of a block (5000 x 5000 um^2) in order to completely align and utilize the maximum area. However, individual chips in the interior account for the maximum area and maintain a minimum 200 um dicing lane with neighboring chips. For instance, for the arrangement method depicted in Figure 1, the reservation-required cutting lane for Chips B and C should be determined based on the boundaries of Chips D and A. In this example, the slanted line area will be wasted and unusable.



(Figure 1)

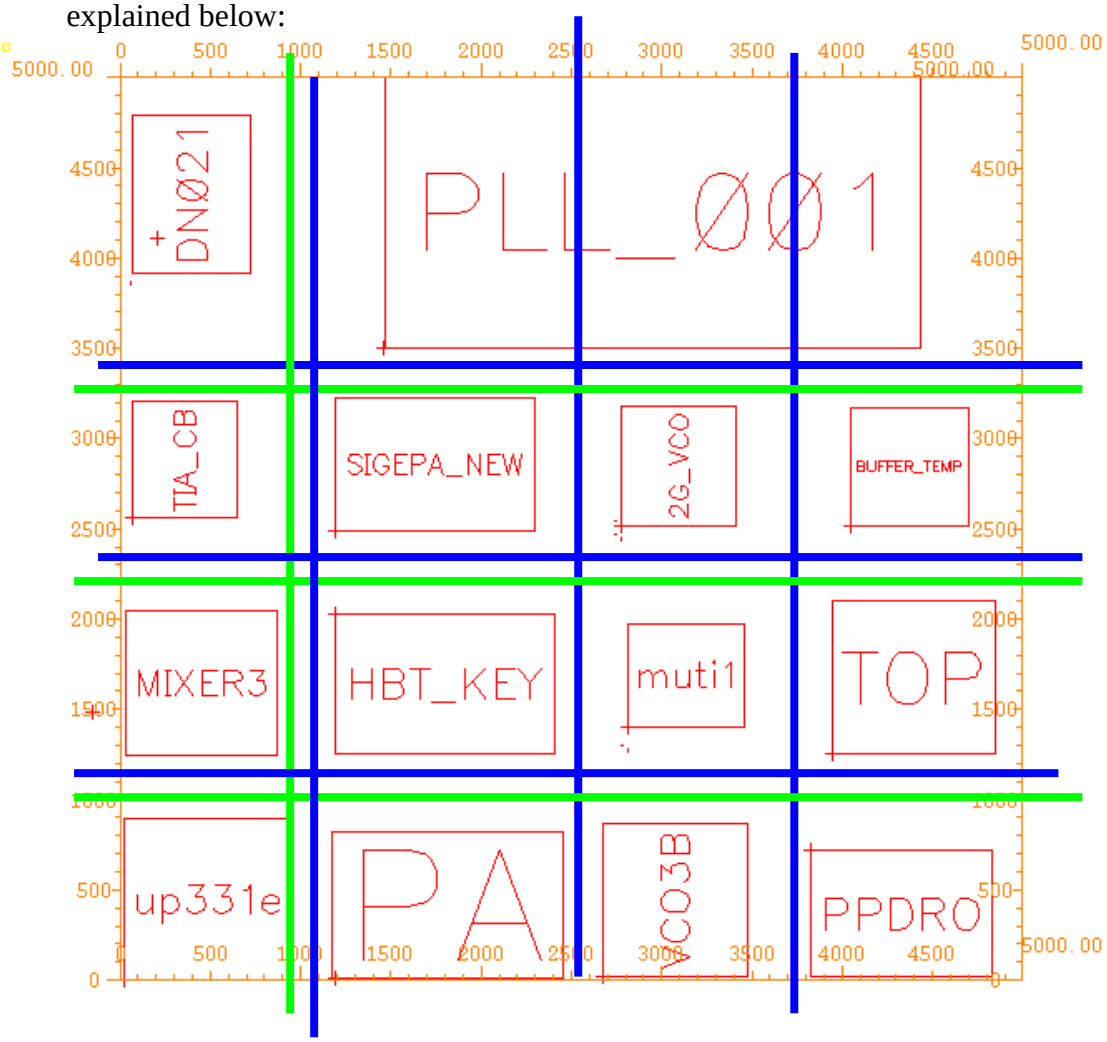
In the layout arrangement, the following techniques and trade-off shall serve as references.

1. Chips with similar area sizes are arranged as closely as possible, or they can be arranged in the same row or same line to maximize area utilization rates. As shown in the first row of Figure 2, the remainder of the area will contain smaller chips.



(Figure 2)

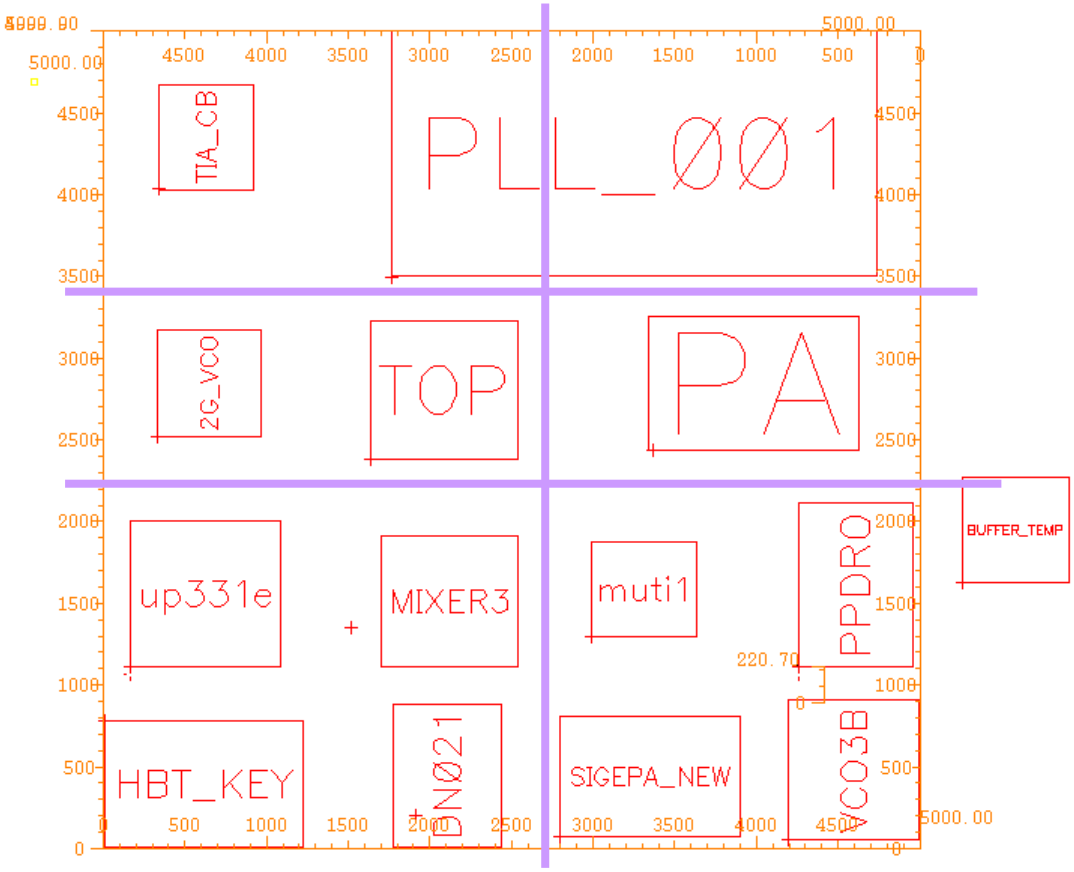
2. When TSRI tapes out TSMC shuttle, each block can obtain 40 brae die. During chip dicing, the dicing method can be designated (i.e. 40 dies can be divided into two or three dicing methods). Therefore, if one or two chips are larger during taping out, their inclusion may fail, or other chips cannot be included. In this case, consider obtaining fewer dies in exchange for all chips tape-out. The example is explained below:



(Figure 3)

As shown in Figure 3, since chip PLL_001 has a larger area, if all chips are to obtain 40 dies, PLL_001 will not be able to tape-out in the configuration. Consider dicing blocks using two distinct methods, such as the blue line sacrificing PLL_001 to obtain additional chips. The green line dicing method involves sacrificing nine chips below PLL_001 in order to obtain PLL_001. Therefore, based on this ratio, it can be determined that, in addition to the chips in the first row, which can obtain a total of 40 dies, the other chips can obtain a maximum of 20 dies.

3. Attempt using rotation method to arrange longer or wider chips together to increase the area utilization rate. As shown in Figure 4, all chips are arranged randomly. It has been discovered that the chip BUFFER_TMP cannot be included in the arrangement. Furthermore, because the chip PA is so large, the entire block requires three dicing methods (including the new purple dicing method) to obtain all chips. This not only wastes space but also results in a smaller number of dies. As a result, chips with similar shapes are flipped and rearranged to find the best arrangement method, as illustrated in Figure 3.



(Figure 4)

As for the way to arrange more than two blocks, the abovementioned technique or method can be used to optimize chip arrangement.