Taiwan Semiconductor Research Institute (TSRI)
Guidelines and Instructions for Applying for advanced chip manufacturing (Including Partial-price , quick review of Partial-price , new faculty discount, superior chip discount.)

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Please view TSRI's Guidelines and Instructions for submitting an application to advanced chip manufacturing. Partial-price, quick review of partial price, new faculty discount, superior chip discount, and other kinds of chips, collectively referred to as advanced chips, are all included in the guidelines and instructions.

Refer to "Item 8 Fee Calculation Details" for details on the fee calculation and amount limit of chip manufacturing, including new faculty discount and superior chip discount. In order to avoid fee calculation issues, users are required to select the correct chip type when submitting a request for chip manufacturing.

Chip manufacturing related information is published on the TSRI's Homepage > News, which is available for viewing.

I. Eligibility for Submission of Chip manufacturing Applications:

Instructors or students under their supervision may submit an application for chip manufacturing if they have obtained the required qualifications for using process technical data from the Technical Standards and Research Institute (TSRI).

II. Application method for process technical data and chip manufacturing:

1. Users are requested to become TSRI members first:
   The website for applying for membership is: http://www.tsri.org.tw/login/login.jsp
2. Complete process technical data application and authorization:
   Instructors may enter the Process/SIP Application webpage (https://www.tsri.org.tw/fab_services/cbs_new.jsp?menu=13&lang=en-US) upon completing membership and log in (http://www.tsri.org.tw/login/login.jsp), or they may visit the website: TSRI > Chip Implementation > Process/SIP Application to submit Process/SIP Application.
3. Prior to applying for chip manufacturing, the user is Requoted to send the following document to the TSRI in advance:
   1) Intellectual Property Rights Affidavit
      Once a year, each instructor will submit the Intellectual Property Rights Affidavit, which can be downloaded from https://www.tsri.org.tw/CommonUtilServlet?type=2.84&file=chipserviced1s1a1englishd1s1a1know_EN.pdf. Professors are asked to finish filling out the documents, sign and seal them, and then email the scanned document files (in PDF or JPG format) to cisd_prouser@narlabs.org.tw.
   2) New Faculty Qualification Inquiry Letter
      Incoming instructors that have served for less than two years shall share no more than seven tape-out chips that have passed review. The total amount of preferential services shall not exceed NT$500,000 (calculated according to the academic community's self-payment). That is, 100% billing is implemented with no additional fees.

      Those that meet qualifications for incoming instructors shall fill out the "New Faculty Qualification Inquiry Letter" (download website: https://www.tsri.org.tw/CommonUtilServlet?type=2.84&file=chipserviced1s1a1englishd1s1a1new_Faculty_EN.pdf), with the department seal affixed and scanned into an electronic file, and sent via email at: cisd_prouser@narlabs.org.tw.

4. Three steps of chip manufacturing applications:

Applicants using processes such as TN7, TN16FFC, TN28HPCplu, TN40G, TN65GP, TN90GUTM, SiGe18, and T18HVG2 are required to complete the following step 1 before 14:00 on the application deadline: fill out the application form and upload the first version of the GDS file (this version of the GDS does not need to be a complete layout or DRC-clean, but the layout area should be as close as possible to the final version). Additionally, Step 2 (upload the final version of the GDS file) and Step 3 should be completed before 14:00 on the deadline for uploading files for Advanced Chip. For advanced quick review chip applications, please complete the upload by 23:59 on the deadline for uploading files for advanced quick review chip.

For applicants using other processes, please complete the following steps1~3 before 14:00 on the application deadline. Late submissions will not be accepted.

Users are asked to visit the following website at https://www.tsri.org.tw/english/chipservice/AETchip.jsp or the TSRI's Homepage > Chip Implementation > Tape-out Guidelines. Refer to the document referenced "Notes on Tape-out Application" on the same webpage. The contains process-specific notes as well as a list of common reasons for application rejection. This will aid users in successfully completing chip manufacturing applications. Please put it to use!

(Step 1) Fill out the Application Form for Chip manufacturing:

After users complete member log in (http://www.tsri.org.tw/login/login.jsp), access the webpage The TSRI's Homepage > Chip Implementation > Tape-out Application > Tape-out New Application, select the correct process MPW Scheduleand chip type and fill out the Application Form for Chip manufacturing.

Note 1: Type of Design Circuit:

For the "design circuit category" items in the "chip information" column of the application form, the applicant must check the correct boxes. The TSRI will organize a review of the same category by the review committee based on the checked category; if a category is not checked or the checks are incorrectly placed, resulting in unfavorable scoring, the applicant bears full responsibility. To avoid disrupting the tape-out schedule, the TSRI will not accept requests for a subsequent review.

Note 2: Research Project of the Ministry of Science and Technology (MOST):

On the application form, the related MOST project names and numbers should be filled out; if there are no related projects, please write "none." However, chip tape-out scheduling has lower priority (compared to application cases with the same ranking of peer review results and total credit).

(Step 2) Upload file data:

After a user logs in as a member, access the web page: TSRI Home Page > Chip Implementation > Tape-out Application > Tape-out Application Summary Table. Before the file upload deadline at 14:00, please upload the following files through the website(For quick review of partial price chips, please upload the files by 23:59 on the deadline). Cases with incomplete application materials will not be accepted.

[1] Design content e-file (sub-file names are limited to *.doc)

[2] GDS file (GDS format)

[3] DRC verification result files

[4] LVS verification result files

[5] Tape-out Review Form

The contents of design content e-files are as follows:

[1] Name and telephone number of the designer. [2] Project name. [3] Most recent three tape-out records. [4] New design or description of revised version.

[5] Current status of relevant research development. [6] Research motivation. [7] Introduction to architecture. [8] Design processes. [9] Simulation results. [10] Measurement considerations.

[11] Description of layout verification result errors. [12] Layout plan. [13] Wire bonding diagram. [14] Estimated Specifications Table. [15] Comparison Table of References. [16] References.

Note 1: **The size of design content e-files is limited to 5MB, the total number of pages is limited to 30 pages, and the preferred image file format is gif**.

Note 2: For design content e-file Item [4] New design or description of revised version, specifically the design case application submitted, select and provide pertinent explanations using the three categories below:

(1) The designer's new design; (2) a revision of an earlier design completed by the designer; and (3) the adoption of another designer's design for improvement.

- If the design falls under (1) the designer's new design, the existing design will not be revision. Please specify "This case is the designer's new design" in Item [4] New design or description of revised version.

- If the design falls under (2) a revision of an earlier design completed by the designer or (3) the adoption of another designer's design for improvement, please specify "This case is a revision of an earlier design completed by the designer" or "This case is the adoption of another designer's design for improvement" in Item [4] New design or description of revised version. The need for a tape-out revision, the specifications of previous tape-out versions, and measurement results should be clarified. In addition, the content of the current revision and the improved specifications should be explained (if the measurement results of the previous version are not normal, the reason chips fail to act normally should be analyzed in order to achieve better results during reviews).

Note 3: Attach the Pre-Layout Simulation and Post-Layout Simulation Comparison Chart to [9] Simulation Results and [14] Estimated Specifications Table in the design content e-file. Reference design content samples for respective specifications should be included in [14] Estimated Specifications Table. In the absence of compliance, the application will not be accepted.

Note 4: Information pertaining to the size of the layout area may not be specified for [12] Layout Plan and other items in the design content e-file. The user has the option of including design case area information in the design content. Due to limitations imposed by the MPW Schedule's overall tape-out and area resources, layout arrangements, and dicing methods, the chip size obtained by the user will differ from the layout area drawn by the user.

(Step 3) Check the uploaded information for completeness and confirm application sending:

(1) After the user logs in as a member, enter the webpage: TSRI Home Page > Chip Implementation > Tape-out Application > Tape-out Application Summary Table. Click the GDS file information button in the application case's GDS file information column and review the layout image and DRC verification results.

(2) Please verify if the application form is complete, that the uploaded file is complete, and that the GDS file information and DRC results are correct. If there are no questions, please submit the

application by clicking the "**Send**" button in the Tape-out Application Summary Table before the deadline.

5. **Users are asked to upload a chip testing report after receiving chips. Refer to Notes Point 13 for specifics.**

III. Process code and description

Process code	Process description
TN7	TSMC 7nm CMOS LOGIC Fin FET ELK Cu 1P17M 0.75/1.8V
TN16FFC	TSMC 16 nm CMOS LOGIC FinFET Compact (Shrink) LL ELK Cu 1P13M 0.8&1.8V
TN28HPCplu	TSMC 28 nm CMOS RF High Performance Compact Mobile Computing Plus (HPC+) ELK Cu 1P10M 0.9&1.8V
TN40G	TSMC 45 nm CMOS LOGIC General Purpose Superb (40G) ELK Cu 1P10M 0.9/2.5V
TN65GP	TSMC 65 nm CMOS Mixed Signal RF General Purpose Plus LowK Cu 1P9M 1.0&2.5V
TN90GUTM	TSMC 90 nm CMOS Mixed Signal MS General Purpose Standard Process LowK Cu 1P9M 1.0&3.3V (With UTM)
T18	TSMC 0.18 um CMOS Mixed Signal RF General Purpose MiM FSG Al 1P6M 1.8&3.3V
U18	UMC 0.18 um Mixed-Mode and RFCMOS 1.8V/3.3V 1P6M Metal Metal Capacitor Process
U18MEMS	UMC 0.18um CMOS and MEMS Process
D35	TSMC 0.35 um Mixed-Signal 2P4M Polycide 3.3/5V
Multi-option-MEMS	TSMC 0.35um CMOS Process and APM MEMS Process wi/wo Gold
SiGe18	TSMC 0.18 um BICMOS Mixed Signal SiGe General Purpose Standard Process FSG Al 3P6M 1.8&3.3V
P15	WIN 0.15 um PHEMT
GaN12	WIN 0.12um RF High Power GaN-on-SiC HEMT Technology
T18HVG2	TSMC 0.18um CMOS HIGH VOLTAGE MIXED SIGNAL BASED GENERATION II BCD 1P6M SALICIDE AL_FSG 1.8/5/6/7/8/12/16/20/24/29/36/45/55/65/70V/VG1.8 /5V AND 5/6/7/8/12/16/20/24/29/36/45/55/65/70V/VG5V
IMEC-SiPh (iSiPP50G)	imec-ePIXfab SiPhotonics: iSiPP50G
IMEC-SiPh (Passives+)	imec-ePIXfab SiPhotonics: passives+
T50GaN	TSMC 0.50 UM GAN WBG E-HEMT USG AL 0P3M HKMG 650V

IV. Notes:

1. The objective of advanced chip manufacturing:
   In principle, it is intended for patent applications and paper publication.
2. Operational processes of advanced chip manufacturing.
   See The TSRI Homepage > Chip Implementation > Tape-out Guidelines for "Advanced Chip manufacturing Application and Review Processes"documents.
3. Chip Manufacturing Service Contact:
   If you have any questions pertaining to application or technical aspects, feel free to contact related business handlers. See the webpage: TSRI Homepage > Chip Implementation > Contact.
4. Update, resubmission, or return of application information:
   After the application deadline, application information updates or resubmission will no longer be accepted to avoid not reviewing operations on time. Applicants who submit insufficient information will not be accepted. Before submitting the application, the applicant must thoroughly inspect the required application information. Application cases that are not accepted will not be returned.

5. TSRI Result Meeting:
   Applicants of papers published for chip manufacturing processes provided by the TSRI (free or partial price manufacturing) are obligated to attend and report at result meetings held by TSRI.
6. Total Credit:
   Total credit = chip credit + service credit + new professor credit
   1) Chip credit = (number of papers in the recent three years)/(number of chips in the recent two years);
      Paper calculation: Journal-Paper(domestic and foreign)*2, Conference-Paper(domestic and foreign)*1, Patent(domestic and foreign)*1, technical transfer (domestic and foreign)*1.
      This year continues to focus on promoting the publication of papers, with the only difference being between the journal and conference fields. To move toward a focus on high-quality research and paper publications, various types of papers of varying weights will be introduced in the future.
      Note: The number of chips in the recent two years excludes the number of chips two years before the current year.

   2) Service Credit:
      School professors who serve as a chip manufacturing reviewer responsible for written reviews and reviews requiring personal attendance will gain service credit.
      Service Credit = (Review meeting attendance count in the previous year + Number of written reviews) * 0.02
      Note: The maximum service credits are 0.2.
   3) New Professor Credit:
      In the last three years, those with fewer than three chips have been designated as new professors, with a uniform total credit of 0.2.
   4) Usage of "total credits":
      When the chip rating is the same level, chip manufacturing is ranked based on the total credits, from higher to lower priority.
7. Acknowledgment for TSRI:
   Papers published for chip manufacturing processes provided by the TSRI should include a reference to the TSRI. Papers that have been published should be registered on the TSRI website: TSRI Homepage > Chip Manufacturing > Total Credit > Performance Filling and Reporting (Paper Registration) Function in order to update total credit information. Professors can update their papers on the TSRI website at any time.
   Examples of Acknowledgement Content for Reference:
   Example 1: This research was supported in part by _____ services from Taiwan Semiconductor Research Institute (TSRI), Taiwan, R.O.C.
   Example 2: The authors would like to acknowledge chip manufacturing support provided by Taiwan Semiconductor Research Institute (TSRI), Taiwan, R.O.C.
8. Multi-option-MEMS:
   The Application Guidelines for Process Chip Manufacturing is the same as those of D35 process chips. Since the wafers for multi-option-MEMS process chips require post-process handling, it takes about 11 weeks.
9. Area Restrictions of Advanced Chips in P15 and GaN12 Processes:
   1mm*1mm / 1mm*2mm / 1.5mm*1mm / 1.5mm*2mm / 2mm*1mm / 2mm*2mm / 2.5mm*1mm / 2.5mm*2mm / 3mm*1mm / 3mm*2mm / 3mm*3mm / 3mm*4mm (other areas will not be accepted.)
10. Area restrictions of IMEC-SiPh (iSiPP50G) process chips:

The allowable areas for tape-out design include: 2.5×2.5 mm^2, and 2.5×5.15 mm^2. Please select one for design use(the overall open status will be adjusted based on the usable area).

11. Area restrictions of IMEC-SiPh (Passives+) process chips:
The allowable areas for tape-out design include: 5.15×2.5 mm^2, and 5.15×5.15 mm^2. Please select one for design use(the overall open status will be adjusted based on the usable area).

12. Number of chips:
From TSRI's organized chip manufacturing, 18 unpackaged chips can be obtained; for chips requiring packaging, eight packaged chips and 10 unpackaged chips can be obtained. Select IMEC-SiPh processes to receive approximately 10 unpackaged chips (exact quantity is dependent on design area and process manufacturer delivery).

13. **Users are asked to upload a chip testing report after receiving chips:**
    1) Method for uploading test reports:
    Users must perform chip testing within two months of receiving (packaged) chips. A test report for the chips, as well as English versions of the test report, should be uploaded as e-files. The TSRI retains the right to utilize the report and summary. After completing member login, users can access the webpage listed below to upload their test report: TSRI Homepage > Chip Implementation > Test Report.
    2) Effects of Delaying Test Report Upload:
    Applications for advanced chip manufacturing by chip designer or students of advisors will not be accepted if a chip designer delays sending of any test report or advisors delay sending of three test reports for advanced chips (including test components). Users may visit the TSRI webpage: TSRI Homepage > Chip Implementation > Test Report Search Test Report Deficiency Status.

14. Each application case corresponds to a design and a GDS file for advanced or educational chips that do not have fixed chip areas that require reviews; the GDS file of the application case may only contain one circuit. A GDS file containing circuit sets that compare performance or functions will not be accepted, nor will chip manufacturing applications containing multiple independent circuits.

V. The advanced chip manufacturing case review method is explained below:
For the quick review of partial price chips, the TSRI implements an internal review process in order to promptly identify artificially paid chips. Following the approval of the quick review of partial price chips, an expedited review of the same as educational chips will ensue. Automatically, the performance of cases that have been approved will be assigned a grade of C (recommended with Reservation). The following procedures facilitate quick review of partial price chips:

1) Chips that use D35, T18, U18, T18HVG2, or T50GaN.
In regard to two distinct categories of chips—partial price and new faculty discount—participation in a review meeting or submission of a written review is permissible. The diverse methods of review are detailed below:

1. Written review:
Individuals whose respective processes satisfy the subsequent criteria are eligible to utilize the written review method:
    1) Application cases that use TN65GP or TN90GUTM process, chip area is < 1 (mm^2).
    2) The written review mechanism is exclusively furnished for use cases involving processes such as T18, U18, D35, SiGe18, T18HVG2, P15, GaN12, IMEC-SiPh, or T50GaN.

TSRI shall transmit the electronic versions of the "Application Form E-file" that applicants submit to the review committee for examination. (Design data submitted should be detailed in order to facilitate a single-sided discussion, without the opportunity for back-and-forth discussions and consultations.)

2. Attend a review meeting:

Those who meet 1) or 2) below will attend a review meeting.

1) Those who do not meet the written review and review exemption application criteria, or those who attend a review meeting voluntarily.
2) Advanced chip application cases that use TN7, TN16FFC, TN28HPCplu, or TN40G processes the falling under the review exempt classification are all required to attend a review meeting.
3) Those who useT18, U18, D35, SiGe18, T18HVG2, P15, GaN12, IMEC-SiPh, or T50GaN processes will not be provided with a review meeting's review mechanism.

To ensure the fairness of review meetings, designers who attend to report are required to comply with identification verification procedures at the review venue. Designers who attend a review meeting must bring two forms of identification: one to exchange for an ID to enter the TSRI building, and the other to verify identity with venue staff prior to reporting.

VI. Review Grade Rating and the Priority of Chip Manufacturing:

1. The priority order of advanced chip manufacturing is as follows:
   1) Chip manufacturing cases rated as grade A (highly recommended) after review.
   2) For chip manufacturing cases rated as grade B (recommended) after review, chips with the same grade are ranked based on the total credits, from higher to lower priority. Then, based on the available space remaining after ranking grade A chips in order, determine whether or not chips can be included in production.
   3) For chip manufacturing cases rated as grade C (recommended with Reservation) after quick review of partial price, chips with the same grade are ranked based on the total credits, from higher to lower priority. Then, based on the remaining usable space after sorting grade A and grade B chips in ascending order, determine whether chips can be included in production.
   4) For chip manufacturing cases rated as grade D (based on the remaining area of wafers with manufacturing tape-out) after review, chips with the same grade are ranked based on the total credits, from higher to lower priority. Then, based on the remaining attainable area after ranking grade A, grade B, and grade C chips and educational chips in order, determine if chips can be included in production.

   Chip manufacturing cases with the same grade are ranked based on the total credits, from higher to lower priority. For processes produced using the shuttle method, in order to avoid some instructors from crowding other instructors' opportunity to have project production cases under their supervision from going tape-out due to the many topic production cases they supervise, the TSRI will rank project production cases supervised by the same instructor and production cases with the same rating after the advanced chip review results have been released; these will be arranged as three for every rotation and are ranked based on the professors' total credits, from higher to lower priority. In order to achieve the best resource use, for instructors with a higher number of projects under their supervision, the second and third round of tape-out scheduling will also be provided until the usable area has been used up, or all the advanced chips for the chip instructor have been included. There is no limit on the number of chips going tape-out for every instructor; after review, chips rated as grade F will not be provided with chip manufacturing services.

2. Principles for chip modification after a advanced chip review:

1) Regardless of what grade advanced chips are under (A,B,C,D), replies (modifications or explanations) should be made according to the review comments of all reviewers (including modifications/recommendations).
2) If reviewers suggest the layout be modified, the length and width of the new layout must not be longer than the original layout. Non-compliant modified new layout files will not be adopted.

3. Chip tape-out scheduling:

Chip tape-out is arranged for manufacturing in accordance with the above-mentioned sequencing standard (For chips rated as levels A,B,C, and D, the TSRI reserves the right to flexibly adjust tape-out.) until the MPW Schedulearea is depleted. Following that, the TSRI will release tape-out data. Chips that are unable to be arranged for manufacturing, regardless of their rated level, will not be retained for manufacturing in the following MPW Schedule.

VII. Announcement:

Upon application deadline and review processing completion, the TSRI will announce unaccepted, accepted, exempted review, and written review application cases via e-mail and on its website. The TSRl will also post an announcement on its website on the Thursday of the review meeting week for application cases that are required to attend a review meeting. In review results, for chip manufacturing application cases (regardless of level), the reviewers are required to complete design modifications **prior to the review committee reply deadline** (refer to the TSRI website's "review result report" under "real-time information" for the actual schedule and complete design modification for chip manufacturing). Chip manufacturing will not be granted for overdue items.

VIII. Fee Calculation Details:

- In order to protect the rights of all users and ensure the efficient use of scarce chip manufacturing resources, the fee collection for partial price chips and quick review of partial price chips in cash will be calculated based on the actual area used, and packaging. Preferential offers for self-payment by the academic community: Payment collection is based on 80% of the announced list price (i.e. list price x 80%). **Preferential offers for partial payment** by the academic community: Payment collection is based on 10% of announced self-payment by the academic community (i.e. list price x 80% x 10%).

  Refer to "Guidelines and Descriptions of Partial Payment by the Academic Community" on the TSRI's chip system "Price List" webpage for information regarding partial payment. Website: https://www.tsri.org.tw/custservice/chip_charges.jsp "Price List";

  For the Guidelines and Instructions for Fee servicer method and Payment, refer to the chip systems price list webpage: https://www.tsri.org.tw/english/chipservice/chip_charges.jsp.

- **Superior chip discount**: Professors that meet superior chip award qualifications will be entitled to 100% billed chip manufacturing preferential services for tape-out chips with the following amount limit from August 1 in the current year to July 31 the following year. Based on the priority of chip manufacturing applied with the following amount limit, which is the chip manufacturing priority rated as Class A (highly recommended).

1. Special award/ISSCC papers: Chip manufacturing services in accordance with the academic community's self-payment total of NT$1 million and the total upper limit of 14 chips.
2. Excellence Award: Chip manufacturing services in accordance with the academic community's self-payment total of NT$400,000 and the total upper limit of 7 chips.
3. Distinction Award: In accordance with the academic community's self-payment total of NT$200,000 million and

the total upper limit of 4 chips.

When using “superior chip discount” Tape-out Applications, payments must be made in full based on the amount limit for superior chip discount; if the remaining amount limit is insufficient to cover the single case (chip) manufacturing fee, the following method of handling must be used.

File a chip manufacturing application using “superior chips” and calculate the total amount based on the academic community’s self-payment. The system will automatically deduct the remaining amount limit of the superior chip discount. The remaining fees will be calculated based on the academic community’s partial payment.

A test report must be submitted for all chip manufacturing applications for “superior chips.”

For designers of superior chips under the same professor (including co-designers), an upper limit in total of NT$150,000 per student and NT$300,000 for two students, and so on.

- **New faculty discount:** Incoming instructors who have not served for two full years are entitled to preferential services of up to seven tape-out chips per year for a total of NT$500,000 (calculated based on self-payment of the academic community). That is, 100% billing is implemented with no additional fees.

Those that meet the qualifications for incoming instructors shall fill out the “New faculty Qualification Inquiry Letter” before applying for the first chip manufacturing (download website: https://www.tsri.org.tw/CommonUtilServlet?type=2.84&file=chipserviced1s1a1englishd1s1a1new_Faculty_EN.pdf). After affixing the department seal and scanning into an e-file, e-mail it to cisd_prouser@narlabs.org.tw.

1. Chip manufacturing : a small area

Process code	Unit price (NTD/mm^2)
TN7	Please refer to the “External Service Collection Method and Description” section of the “Price List” webpage for TSRI’s chip system. The “Price List” webpage contains the following information: https://www.tsri.org.tw/english/chipservice/chip_charges.jsp
TN16FFC	
TN28HPCplu	
TN40G	
TN65GP	
TN90GUTM	
T18	
U18	
U18MEMS	
D35	
Multi-option-MEMS	
SiGe18	
P15	
GaN12	
T18HVG2	
IMEC-SiPh (iSiPP50G)	
IMEC-SiPh (Passives+)	
T50GaN	

2. Chip manufacturing : Large Area (1 Block)

Process code	Unit price (NTD/block)	Remarks
TN7	Please refer to the “External Service Collection Method and Description” section of the “Price List” webpage for TSRI’s chip system. The “Price List” webpage contains the following information: https://www.tsri.org.tw/english/chipservice/chip_charges.jsp	MPW, Block=（2mm^2）
TN16FFC		MPW, Block =（4 mm^2）
TN28HPCplu		MPW, Block =（6 mm^2）
TN40G		MPW, Block =（9 mm^2）
TN65GP		MPW, Block=（12mm^2）
TN90GUTM		MPW, Block=（16mm^2）
T18		Full Wafer, Block=（25mm^2）
U18		Full Wafer, Block=（25mm^2）
U18MEMS		Full Wafer, Block=（25mm^2）
D35		Full Wafer, Block=（25mm^2）
Multi-option-MEMS		Full Wafer, Block=（25mm^2）
SiGe18		MPW, Block=（25mm^2）
T18HVG2		MPW, Block =（25 mm^2）
IMEC-SiPh (iSiPP50G)		1 minblock= 6.25mm^2
IMEC-SiPh (Passives+)		MPW, Half Block= 12.875mm^2
IMEC-SiPh (Passives+)		MPW, Block= 26.5225mm^2

3. Chip packaging

The unit price of packaging is the cost of packaging one chip. From TSRI's organized chip manufacturing requiring packaging, eight packaged chips can be obtained.

Type	Unit price (NTD/chip)
S/B-18	Please refer to the "External Service Collection Method and Description" section of the "Price List" webpage for TSRI's chip system. The "Price List" webpage contains the following information: https://www.tsri.org.tw/english/chipservice/chip_charges.jsp
S/B-24	
S/B-28	
S/B-32	
S/B-40	
S/B-48	
CQFJ-68	
CQFJ-84	
CQFP-100	
CQFP-128	
CQFP-144	
CQFP-160	
CQFP-208	