Taiwan Semiconductor Research Institute (TSRI)
Guidelines and Instructions for Applying for Educational Chip Manufacturing

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Feel free to view TSRI's Guidelines and Instructions for Applying for Educational Chip Manufacturing.

Chip manufacturing related information is published on the TSRI's Homepage > News, which is available for viewing.

I. Explanation of Objectives and Application Summary:

Educational chip manufacturing services are designed for educational training purposes. Prior to accessing process technology information related to educational chip manufacturing through the TSRI, instructors from various domestic academic institutions must first obtain qualifications for using the process technology data (refer to references two and three). Students enrolled in their courses may submit chip manufacturing applications related to course content during the effective MPW Schedule in which they have obtained technical data access qualifications (refer to Item 4-1 for details). Each student in a course is allowed to proceed with chip manufacturing only once per course. The choice of process and run is a collaborative decision between the instructing teacher and the students, and the educational chip manufacturing application is submitted by the enrolled students.

II. Process code and description of educational chip manufacturing services:

Process code	Process description
TN65GP	TSMC 65 nm CMOS Mixed Signal RF General Purpose Plus LowK Cu 1P9M 1.0&2.5V
TN90GUTM	TSMC 90 nm CMOS Mixed Signal MS General Purpose Standard Process LowK Cu 1P9M 1.0&3.3V (With UTM)
T18	TSMC 0.18 um CMOS Mixed Signal RF General Purpose MiM FSG Al 1P6M 1.8&3.3V
U18	UMC 0.18 um Mixed-Mode and RFCMOS 1.8V/3.3V 1P6M Metal Metal Capacitor Process
U18MEMS	UMC 0.18um CMOS and MEMS Process
D35	TSMC 0.35 um Mixed-Signal 2P4M Polycide 3.3/5V
Multi-option-MEMS	TSMC 0.35um CMOS Process and APM MEMS Process wi/wo Gold
SiGe18	TSMC 0.18 um BICMOS Mixed Signal SiGe General Purpose Standard Process FSG Al 3P6M 1.8&3.3V
P15	WIN 0.15 um PHEMT
GaN12	WIN 0.12um RF High Power GaN-on-SiC HEMT Technology
T18HVG2	TSMC 0.18um CMOS HIGH VOLTAGE MIXED SIGNAL BASED GENERATION II BCD 1P6M SALICIDE AL_FSG 1.8/5/6/7/8/12/16/20/24/29/36/45/55/65/70V/VG1.8/5V AND 5/6/7/8/12/16/20/24/29/36/45/55/65/70V/VG5V
T50GaN	TSMC 0.50 UM GAN WBG E-HEMT USG AL 0P3M HKMG 650V

III. Application method for process technical data and chip manufacturing:

1. Users are requested to become TSRI members first:
   The website for applying for membership is: http://www.tsri.org.tw/login/login.jsp
2. Complete process technical data application and authorization:
   Instructors may enter the Process/SIP Application webpage (https://www.tsri.org.tw/fab_services/cbs_new.jsp?menu=13&lang=en-US) upon completing membership and log in (http://www.tsri.org.tw/login/login.jsp), or they may visit the website: TSRI Chip Implementation > Process/SIP Application to submit Process/SIP Application.
3. Prior to applying for chip manufacturing, the user is Requoted to send the following information to the TSRI in advance:
   1) Intellectual Property Rights Affidavit

Once a year, each instructor will submit the Intellectual Property Rights Affidavit, which can be downloaded from https://www.tsri.org.tw/CommonUtilServlet?type=2.84&file=chipserviced1s1a1englishd1s1a1know_EN.pdf. Professors are asked to finish filling out the documents, sign and seal them, and then email the scanned document files (in PDF or JPG format) to cisd_prouser@narlabs.org.tw.

2) Score list and course list in Excel format files

Prior to applying for educational chip manufacturing, professors are required to: https://www.tsri.org.tw/CommonUtilServlet?type=2.84&file=chipserviced1s1a1englishd1s1a1edu_EN.xls download the form. Once the form has been completed, please send an email containing the completed form (Excel file) and a scanned copy of the course's score list (including the department seal and the course professor's signature in PDF or image file format) to: cisd_edu@narlabs.org.tw; Only one submission per course is mandatory.

4. Three steps of chip manufacturing applications:

Applicants using processes such as TN65GP, TN90GUTM, SiGe18, and T18HVG2 must complete the following steps 1 before 14:00 on the application deadline: fill out the application form and upload the first version of the GDS file. (This GDS version does not need to be a complete layout or DRC-clean, but please ensure that the layout area is as close as possible to the final version.)
Additionally, before the Deadline for uploading files for Educational Chip (by 14:00), please complete Step 2 (upload the final version of the GDS file) and Step 3.
For applicants using other processes, please complete the following steps1~3 before 14:00 on the application deadline. Late submissions will not be accepted.

Users are asked to visit the following website at https://www.tsri.org.tw/english/chipservice/AETchip.jsp or the TSRI's Homepage > Chip Implementation > Tape-out Guidelines. Refer to the document referenced "Notes on Tape-out Application" on the same webpage. This contains process-specific notes as well as a list of common reasons for application rejection. This will aid users in successfully completing chip manufacturing applications. Please put it to use!

(Step 1) Fill out the Application Form for Chip manufacturing:

After users complete member log in (http://www.tsri.org.tw/login/login.jsp), enter the webpage: The TSRI's Homepage > Chip Implementation > Tape-out Application > New Tape-out Application, select the correct process MPW Schedule and chip type and fill out the Application Form for Chip Manufacturing.

(Step 2) Upload file data:

After the user logs in as a member, access the webpage: TSRI Home Page>Chip Implementation > Tape-out Application > Tape-out Application Summary Table. Before the application deadline, upload the file below via the webpage. Incomplete application case files will not be accepted.

[1] Design content e-file (sub-file names are limited to *.doc)
[2] GDS file (GDS format)
[3] DRC verification result files
[4] LVS verification result files
[5] Tape-out Review Form

The contents of design content e-files are as follows:
[1] Name and telephone number of the designer. [2] Project name. [3] New design or description of revised version. [4] Description of principles and architecture description. [5] Design process. [6] Circuit drawing.

[7] Simulation results. [8] Measurement considerations. [9] Description of layout verification result errors. [10] Layout plan. [11] Wire bonding diagram. [12] Estimated Specifications Table. [13] References.

Note 1: **The size of design content e-files is limited to 5MB, the total number of pages is limited to 30 pages, and the preferred image file format is gif**.

Note 2: For design content e-file Item [3] New design or description of revised version, specifically the design case application submitted, select and provide pertinent explanations using the three categories below:
(1) The designer's new design; (2) a revision of an earlier design completed by the designer; and (3) the adoption of another designer's design for improvement.
- If the design falls under (1) the designer's new design, the existing design will not be revision. please specify "This case is the designer's new design" in Item [3] New design or description of revised version;
- If the design falls under (2) A revision of a previously completed design by the designer; or (3) Utilization of another designer's design with modifications, please specify "This case is a revision of an earlier design completed by the designer" or "This case is the adoption of another designer's design for improvement" in Item [3] New design or description of revised version. Also explain why revision and tape-out are required, past tape-out version specifications and measurement results, an explanation of the contents of the revision, the specifications improved, and other information (If previous version measurement results indicate abnormal behavior, it is necessary to investigate the causes of chips not operating normally.)

Note 3: Attach the Pre-Layout Simulation and Post-Layout Simulation Comparison Chart to [7] Simulation Results and [12] Estimated Specifications Table in the design content e-file. Reference design content samples for respective specifications should be included in [12] Estimated Specifications Table. In the absence of compliance, the application will not be accepted.

Note 4: The size of the layout area may not be specified for [10] Layout Plan and other elements in the design content e-file. The user has the option of including design case area information in the design content. Due to limitations imposed by the MPW Schedule's overall tape-out and area resources, layout arrangements, and dicing methods, the chip size obtained by the user will differ from the layout area drawn by the user.

(Step 3) Check the uploaded information for completeness and confirm application sending:

(1) After the user logs in as a member, enter the webpage: TSRI Home Page > Chip Implementation > Tape-out Application > Tape-out Application Summary Table. Click the GDS file information button in the application case's GDS file information column and review the layout image and DRC verification results.

(2) Please verify if the application form is complete, that the uploaded file is complete, and that the GDS file information and DRC results are correct. If there are no questions, please submit the application by clicking the "**Send**" button in the Tape-out Application Summary Table before the deadline.

5. **Users are asked to upload a chip testing report after receiving chips. Refer to Notes Point 10 for specifics.**

IV. Notes:

1. Effective time of application of educational chip manufacturing and explanation of ranking principles:
In order to provide the designer with adequate time to get familiar with the environment and complete related design, students taking courses in the first semester are requested to apply for educational chip

manufacturing from the period of course commencement to September of the following year (see explanation in Item 3-3) after the professor sends the necessary documents; students taking courses in the second semester are requested to apply for educational chip manufacturing after the professor sends the necessary documents from the period of course commencement to the end of March the following year (see explanation in Item 3-3). Log in to the TSRI's website to search the validity period of tape-out status of students' educational chip applications. After logging in to the TSRI website, enter Process Services > Tape-out Applications > View Tape-out Eligibility > 3. Educational chip tape-out records to search.

When multiple educational chips are used in the current MPW Schedule, the professor is asked to independently evaluate the tape-out priority based on each course, which will be used as a reference during the TSRI review. The TSRI will determine the preferred manufacturing quantity based on the amount of photomask area and educational chip review.

In order to prevent some courses from overshadowing opportunities for students in other courses due to a large number of application cases, the TSRI will rank each course, prioritizing the arrangement of one to three chips per round. Students enrolled in the course will be able to use educational chip tape-out in this manner. To maximize resource utilization, the second and third rounds of tape-out scheduling are also provided to courses with more student application cases until all usable areas are depleted or all educational chips have been arranged. There is no tape-out chip limit, with the hope that the majority of students will receive complete training.

Because educational chip designers are newcomers to the field of IC design, the TSRI will add an educational chip modification layout mechanism after the deadline to avoid application case rejection due to DRC errors and other layout issues, resulting in missed opportunities for chip implementation and subsequent chip measurement. Please keep an eye out for notifications after the application deadline.

2. Operational processes of educational chip manufacturing:
   Seethe TSRI's Homepage > Chip Implementation > Tape-out Guidelines "Educational Chip Manufacturing Applications and Review Processes" Documents

3. Chip Manufacturing Service Contact:
   If you have any questions pertaining to application or technical aspects, feel free to contact related business handlers. See the webpage: TSRI Homepage > Chip Implementation > Contact.

4. Update, resubmission, or return of application information:
   After the application deadline, application information updates or resubmission will no longer be accepted to avoid not reviewing operations on time. Applicants who submit insufficient information will not be accepted. Before submitting the application, the applicant must thoroughly inspect the required application information. Application cases that are not accepted will not be returned.

5. TSRI Result Meeting:
   Applicants of papers published for chip manufacturing processes provided by the TSRI (free or partially self-funded manufacturing) are obligated to attend and report at result meetings held by TSRI.

6. Total Credit:
   Total credit = chip credit + service credit + new professor credit

   1) Chip credit = (number of papers in the recent three years)/(number of chips in the recent two years);
      Paper calculation: Journal-Paper(domestic and foreign)*2, Conference-Paper(domestic and foreign)*1, Patent(domestic and foreign)*1, technical transfer (domestic and foreign)*1.
      This year continues to focus on promoting the publication of papers, with the only difference being between the journal and conference fields. To move toward a focus on high-quality research and paper publications, various types of papers of varying weights will be introduced in the future.
      Note: The number of chips in the recent two years excludes the number of chips two years before the current year.
   2) Service Credit:

School professors who serve as a chip manufacturing reviewer responsible for written reviews and reviews requiring personal attendance will gain service credit.

Service Credit = (Review meeting attendance count in the previous year + Number of written reviews) * 0.02

Note: The maximum service credits are 0.2.

3) New Professor Credit:

In the last three years, those with fewer than three chips have been designated as new professors, with a uniform total credit of 0.2.

4) Usage of "total credits":

When the chip rating is the same level, chip manufacturing is ranked based on the total credits, from higher to lower priority.

7. Acknowledgment for TSRI:

Papers published for chip manufacturing processes provided by the TSRI should include a reference to the TSRI. Papers that have been published should be registered on the TSRI website: TSRI Homepage > Chip Manufacturing > Total Credit > Performance Filling and Reporting (Paper Registration) Function in order to update total credit information. Professors can update their papers on the TSRI website at any time.

Examples of Acknowledgement Content for Reference:

Example 1: This research was supported in part by _____ services from Taiwan Semiconductor Research Institute (TSRI), Taiwan, R. O. C.

Example 2: The authors would like to acknowledge chip fabrication support provided by Taiwan Semiconductor Research Institute (TSRI), Taiwan, R. O. C.

8. The educational chip manufacturing area limit in respective processes:

D35/Multi-option-MEMS: The area must be less than or equal to 1.5*1.5 (mm^2), and the single-side length must not exceed 1.5mm.

T18HVG2: The area must be less than or equal to 1.3*1.3 (mm^2), and the single-side length must not exceed 1.3mm.

T18: The area must be less than or equal to1.2*1.2 (mm^2), and the single-side length must not exceed 1.2mm.

U18 / U18MEMS18: The area must be less than or equal to 1.5*1.5 (mm^2), and the single-side length must not exceed 1.5mm.

TN90GUTM: The area must be less than or equal to 1*1 (mm^2), and the single-side length must not exceed 1mm.

TN65GP: The area must be less than or equal to 0.8*0.8 (mm^2), and the single-side length must not exceed 0.8mm.

T50GaN: The area must be less than or equal to 1.2*1.2 (mm^2), and the single-side length must not exceed 1.2mm.

SiGe18: The area must be less than or equal to 1.2*1.2 (mm^2), and the single-side length must not exceed 1.2mm.

P15: The area (X*Y) must be equal to any of the following areas: 1mm*1mm / 1mm*2mm / 1.5mm*1mm / 1.5mm*2mm / 2mm*1mm / 2.5mm*1mm / 3mm*1mm.

GaN12: The area (X*Y) must be equal to 1mm*1mm.

9. Number of chips:

From TSRI's organized chip manufacturing, 18 unpackaged chips can be obtained; for chips requiring packaging, 2 packaged chips and 16 unpackaged chips can be obtained.

10. **Users are asked to upload a chip testing report after receiving chips:**

1) Method for uploading test reports:
Users must perform chip testing within two months of receiving (packaged) chips. A test report for the chips, as well as English versions of the test report, should be uploaded as e-files. The TSRI retains the right to utilize the report and summary. After completing member login, users can access the webpage listed below to upload their test report: TSRI Homepage > Chip Implementation > Test Report.

2) Effects of Delaying Test Report Upload:
Applications for advanced chip manufacturing by IC designer or students of advisors will not be accepted if the chip designer delays uploading any test report, or the uploading of six educational chip test reports under the professor's name is delayed. Users may visit the TSRI webpage: TSRI Homepage > Chip Implementation > Test Report Search Test Report Deficiency Status.

11. Each application case corresponds to a design and a GDS file for advanced or educational chips that do not have fixed chip areas that require reviews; the GDS file of the application case may only contain one circuit. A GDS file containing circuit sets that compare performance or functions will not be accepted, nor will chip manufacturing applications containing multiple independent circuits.

V. Review basis:

The completeness of design and simulation, the completeness of layout and verification, the repeatability of the same course design title, chip layout area utilization rate, relevance with course content, the integrity of all contents in the application form, overdue test result reports, instructor selection priority.

VI. Priority of educational chip manufacturing:

1. The priority sequence of educational chip manufacturing is as follows:
In order to to prevent some courses from overshadowing opportunities for students in other courses due to a large number of application cases, the TSRI will rank each course, prioritizing the arrangement of one to three chips per round. Students enrolled in the course will be able to use educational chip tape-out in this manner. To maximize resource utilization, the second and third rounds of tape-out scheduling are also provided to courses with more student application cases until all usable areas are depleted or all educational chips have been arranged.

2. Chip tape-out scheduling:
Chip tape-out manufacturing scheduling is in accordance with the aforementioned sequencing standard until the MPW Schedulearea is depleted (the TSRI reserves the right to adjust tape-out as needed). Subsequently, the TSRI will publish tape-out data. Chips that are not scheduled for manufacturing, regardless of rated grade, are not retained for manufacturing in the next MPW Schedule.

VII. Announcement:

After the deadline and after completing review handling, the TSRI will announce whether or not an application case was accepted via email and on the website.

VIII. Fee Calculation Details

The goal is to provide students with complete IC design and implementation training in conjunction with educational chip manufacturing services in school courses. As a result, educational chip procurement is handled by 100% billing with no additional fees.

1. Chip manufacturing

Process code	Unit price (NTD/mm^2)
TN65GP	Please refer to the “External Service Collection Method and Description” section of the “Price List” webpage for TSRI’s chip system. The “Price List” webpage contains the following information: https://www.tsri.org.tw/english/chipservice/chip_charges.jsp
TN90GUTM	
T18	
U18	
U18MEMS	
D35	
Multi-option-MEMS	
SiGe18	
P15	
T18HVG2	
GaN12	
T50GaN	

2. Chip packaging

The unit price of packaging is the cost of packaging one chip. From TSRI’s organized chip manufacturing requiring packaging, **2** packaged chips can be obtained.

Type	Unit price (NTD/chip)
S/B-18	Please refer to the “External Service Collection Method and Description” section of the “Price List” webpage for TSRI’s chip system. The “Price List” webpage contains the following information: https://www.tsri.org.tw/english/chipservice/chip_charges.jsp
S/B-24	
S/B-28	
S/B-32	
S/B-40	