

IPD Process Service Instructions

This Instruction provides users about IPD process information and notices.

All the IPD Process Services follow relevant TSRI Chip Implementation Service Instructions.

1. Process Information:

Process Code	Process Description	Annual Batch No.
WIPD	WIN Integrated Passive Device	2

2. Schedule:

Batch	Application Start Date	Educational Chip Application Deadline	Advanced Chip Application Deadline	Advanced Chip Fast Review Application Deadline	Academia Full-price Application Deadline	Review Meeting	First Stage Approval Deadline	Chip Out	Test Plan Submit Deadline
WIPD-114A	2025.2.3	X	2025.2.10	X	2025.2.17	NA	2025.2.26	2025.6.2	2025.8.8
WIPD-114B	2025.7.28	X	2025.8.4	X	2025.8.11	NA	2025.8.20	2025.11.24	2026.2.6

3. Official Unit Price

Process Code	Unit Price (NTD/mm ²)
WIPD	9,300

Charge methods, please refer to TSRI web document “Chip Implementation / Chip Package Service Charge Methods and Instructions” at web [TSRI > Chip Implementation > Price List](https://www.tsri.org.tw/tw/chipservice/chip_charges.jsp)
https://www.tsri.org.tw/tw/chipservice/chip_charges.jsp

4. Notices:

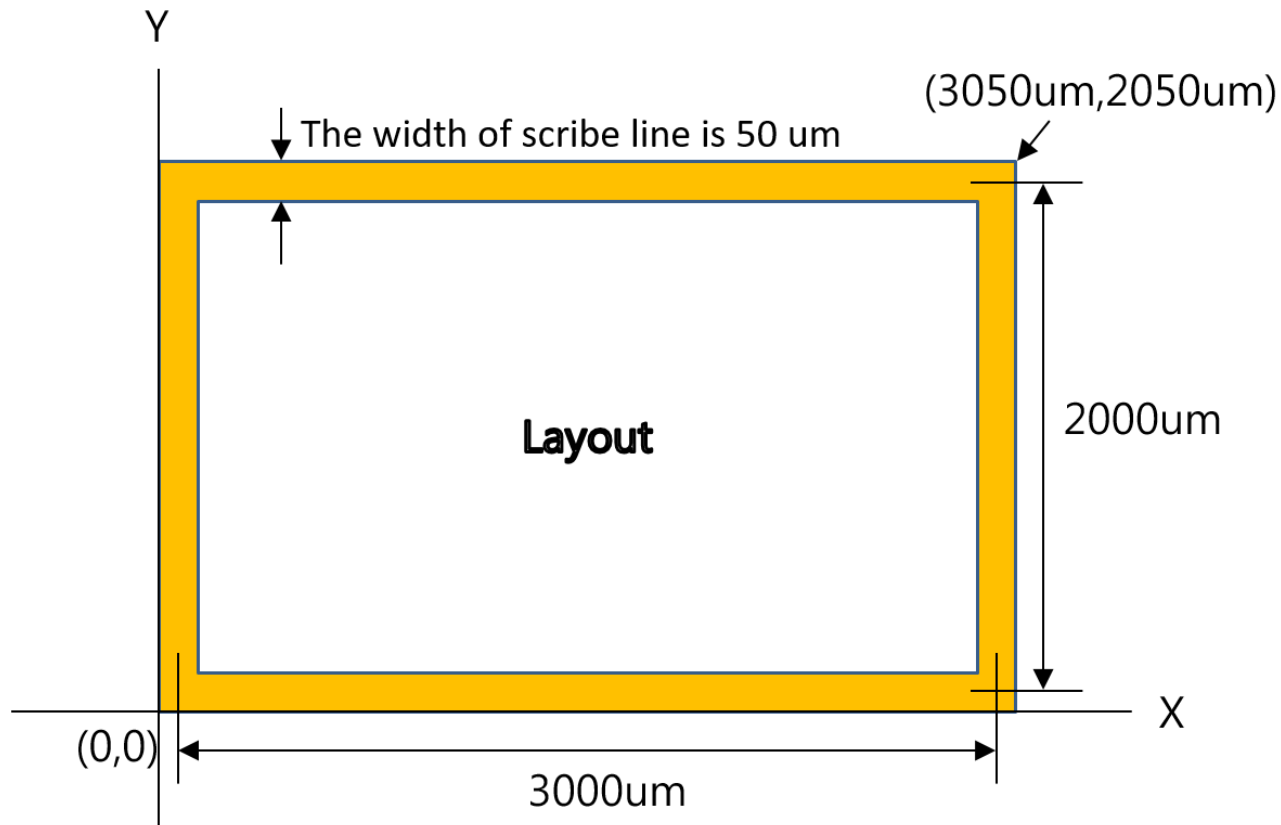
IPD Process

- 1) Please add cutting paths into layout, and make sure that the width of cutting path is 50 um. This regulation means that the available layout area is the interior of the area which surrounded by the cutting paths. The purpose is to preserve the chip cutting paths; the lower left corner should align at origin (0, 0), and the overall layout of the chip should be situated in the first quadrant and comply with the area limit listed below.
- 2) WIPD Process implementation area limit (The distance of the centers of left / right and up / down of cutting paths defines the following fixed area size. There are 19 area size selections. The other area size is not considered for processing. Please refer to the following figure as example.)

1mm*1mm / 1mm*1.5mm / 1mm*2mm / 1mm*2.5mm /
1.5mm*1.5mm / 1.5mm*2mm / 1.5mm*2.5mm / 1.5mm*3mm /
2mm*2mm / 2mm*2.5mm / 2mm*3mm / 2mm*4mm / 2mm*5mm /
3mm*3mm / 3mm*4mm / 3mm*5mm /
4mm*4mm / 4mm*5mm /
5mm*5mm ◦

Example:

The scribe line of 3mm*2mm design application. The diagrammatic sketch of layout.



The distance of the centers of left / right and up / down of scribe line defines the utilized area.

3) To ensure correct output of GDS files, we recommend that the user use the Cadence Virtuoso Layout Editor software to draw the layout.

4) WIPD Process supports ADS and MWO circuit design software. When drawing the layout, the user can use these 2 software

built-in functions to conduct simple DRC (Design Rule Check), but these methods can not finish the complete DRC, only part of DRC. Users must complete Cadence Assura DRC verification procedures before fabrication application. (The recommended parameters setup, please refer to web document: "Assura_Setting_20180321.pdf" at web Chip Implementation > Technical Data Download > Technical Documents, and the link is <https://cms.tsri.org.tw/fab/techfiledownload/init.action>). In order to successfully connect to IC manufacturer's verification procedures, we only accept Assura DRC results.

5) Before application, make sure to use the latest version of PDK layout environment. Because the IC manufacturing company updates Assura DRC verification files frequently, we provide an independent link for the technical file download. Please check the following figure for the link:

技術資料						
請選擇製程：	WIPD,WIN Integrated Pas: ▾					
請選擇下載類型：	<input type="radio"/> 技術文件 <input checked="" type="radio"/> 技術檔案 <input type="radio"/> 應用文件 <input type="radio"/> 測試元件 <input type="radio"/> 矽智財					
為了確保能正常下載技術檔案，建議您使用下列網站瀏覽器。包括：Microsoft Edge、Mozilla Firefox以及 Google Chrome(註)最新版本。註:當您使用的瀏覽器無法下載時,請先暫停使用外掛程式。						
	檔案名稱	檔案簡介	版本	更新日期	修改者	下載
1	PDK_IP3M-00	Process Design Kit of IP3M-00	Rev 1.2. 2.6. 6	2021/09/19	林大業	下載
2	Assura_DRC	Assura DRC command file (最新版本，不定期更新)	v10 4_0 9	2023/03/25	林大業	下載
最前頁 1 ▾ 最後頁 每頁顯示 10 筆 共 2 筆資料						

Flip-Chip Package:

The users may use different item, or batch of any front-end IC processes to apply “IPD Process Application Full-Price Flip-Chip Assembly Service” . If there is any problem, please feel free to contact our designated business personnel.

Contact

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